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TITLE: Memory cell configuration, magnetic ram, and associative memory

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Abstract Text - ABTX (1):

A memory cell configuration has word lines and bit lines that extend transversely with respect thereto. Memory elements with a giant magnetoresistive effect are respectively connected between one of the word lines and one of the bit lines. The bit lines are each connected to a sense amplifier by means of which the potential on the respective bit line can be regulated to a reference potential and at which an output signal can be picked off. The memory cell configuration can be used both as an MRAM and as an associative memory.

Application Filing Date - AD (1):

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Brief Summary Text - BSTX (5):

It has been proposed (see, for example, D. D. Tang et al., IEDM 95, pages 997-99; D. D. Tang et al., IEEE Trans. on Magnetics, Vol. 31, No. 6, 1995, pages 3206-08; F. W. Patten et al., Int. Non Volatile Memory Technology Conf., 1996, pages 1-2) to use such GMR elements as memory elements in a memory cell configuration. For this purpose, GMR elements in which the magnetization direction of one ferromagnetic layer is fixed for example by an adjacent antiferromagnetic layer are used as memory elements. The memory elements are connected in series via bit lines. Word lines run transversely with respect to the latter and are insulated from both the bit lines and the memory elements.

Signals applied to the word lines cause a magnetic field as a result of the current flowing in the word line. The magnetic field influences the memory elements situated underneath. In order to write information, signals are applied to a bit line and a word line, which intersect above the memory cell to be written to. At the point of intersection, the signals cause a magnetic field which is sufficient for the magnetization reversal. In order to read the information, a pulsed signal is applied to the word line. The pulsed signal switches the relevant memory cell back and forth between the two magnetization states. The current through the bit line is measured and the resistance of the corresponding memory element is determined from the measured current. S. Tehrani et al. IEDM 96, pages 193 ff., have proposed using a GMR element having ferromagnetic layers of different thicknesses as the memory element. The magnetic field for writing information is dimensioned such that it only influences the magnetization in the thinner of the two ferromagnetic layers. The magnetization in the thicker of the two ferromagnetic layers remains uninfluenced by it.

Brief Summary Text - BSTX (6):
It is an obvious drawback that the read-out operation with pulsed signals requires an increased outlay on circuitry in these memory cell configurations.

Brief Summary Text - BSTX (8):
It is accordingly an object of the invention to provide a memory cell configuration with GMR elements, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which can be read with a reduced outlay on circuitry.

Brief Summary Text - BSTX (9):
With the foregoing and other objects in view there is provided, in accordance with the invention, a memory cell configuration, comprising: a

plurality of substantially parallel word lines and a plurality of substantially
parallel bit lines running transversely to the bit lines; memory elements
having a layer structure with a giant magnetoresistive effect, the memory
elements being respectively connected between one of the word lines and one of
the bit lines and having a higher resistance than the word lines and the bit
lines; a sense amplifier connected to each of the bit lines for regulating a
potential on a respective the bit line to a reference potential and outputting
an output signal.

Brief Summary Text - BSTX (11):

In other words, the memory cell configuration has word lines bit lines
traversing the word lines. Memory elements having a layer structure with a
very large magnetoresistive effect (GMR), that is to say GMR elements, are
provided. The GMR elements are respectively connected between one of the word
lines and one of the bit lines and have a higher resistance than the word lines
and the bit lines. The bit lines are each connected to a sense amplifier by
means of which the potential on the respective bit line can be regulated to a
reference potential and at which an output signal can be picked off. In order
to read this memory cell configuration, all the word lines which are not
selected are put at the reference potential. A signal with a different
potential is applied to the selected word line. A current path from the
selected word line to all the bit lines is closed as a result of this. The
resistance of the memory element situated at the point of intersection of the
word line with the respective bit line can be determined from the output signal
at the respective sense amplifier, the electrical characteristic parameters of
the sense amplifier, such as the feedback resistance, for example, and the
reference potential and the bit line resistance. A pulsed signal is

not necessary, therefore, in order to read this memory cell configuration.

Brief Summary Text - BSTX (12):

The sense amplifier preferably has a feedback operational amplifier. The non-inverting input of the operational amplifier is connected to reference potential, for example to ground. The bit line is connected to the inverting input. If the reference potential is 0 volts, then this operational amplifier ensures that 0 volts are present on the bit line. The output signal of the operational amplifier is a measure of the resistance of the selected memory element.

Brief Summary Text - BSTX (13):

All known GMR elements are suitable as the memory element, provided that they have a higher resistance than the bit line and the word line in both magnetization states. The GMR effect is greater if the current flows perpendicularly through the layer stack than if the current flows in parallel into the layers.

Brief Summary Text - BSTX (15):

It is advantageous to use an insulating, non-magnetic layer since the GMR effect, which is brought about by a spin-polarized tunneling current through the insulating, non-magnetic layer arranged between the two ferromagnetic layers, is much greater in these structures than if a non-insulating, non-magnetic layer is used. The different resistances assigned to two different logic values 0 and 1 in the memory cell configuration can be better distinguished as a result of this.

Brief Summary Text - BSTX (18):

In order to write information to one of the memory elements, a respective signal is applied to the associated word line and to the associated bit line. As a result, a current flows via the word line and the bit line and induces a

magnetic field in each case. At the point of interception of the word line and
bit line, the total magnetic field resulting from superposition of the two
magnetic fields is large enough to ensure magnetization reversal of the memory
element situated there. Outside the point of intersection, the individual
magnetic fields are too small for magnetization reversal of the memory elements
situated there.

Brief Summary Text - BSTX (19):
In applications where an increased magnetic field is necessary or desirable
for the purpose of writing, it lies within the scope of the invention to
additionally provide write lines running essentially parallel to one another,
which write lines run parallel to the bit lines, for example. These write
lines are insulated from the word lines and the bit lines. By applying a
signal to the corresponding write line, it is possible to amplify the magnetic
field at the point of intersection with the selected word line and thus to
support the writing operation.

Brief Summary Text - BSTX (20):
The memory cell configuration is suitable as a magnetic RAM (MRAM).

Brief Summary Text - BSTX (21):
Furthermore, the memory cell configuration can be operated as an associative
memory. For this purpose, a respective threshold value element is provided
with regard to the bit lines, which element is connected to the output of the
sense amplifier of the respective bit line.

Brief Summary Text - BSTX (22):
In an associative memory, as disclosed for example in K. Goser et al., IEEE
Micro, 9 (1989) 6, pages 28-44, an input signal is applied simultaneously to
all the word lines. The input signal has as many places as word lines. The
current is summed at each of the bit lines and the output signal is

formed with
a threshold value element. In the associative memories disclosed in Goser et
al., IEEE Micro, 9 (1986) 6, pages 28-44, the memory cell comprises only a
conventional resistor or a transistor and is connected between intersecting
word lines and bit lines. These conventional resistors and transistors cannot
be altered during operation, with the result that the memory is not capable of
learning. As an alternative, the memory cells are realized as EEPROM cells,
thereby enabling programming, which are more complicated to fabricate, however.

Brief Summary Text - BSTX (24):
In accordance with a further embodiment of the invention, a differential
amplifier is provided with regard to two bit lines in each case. The inputs of
the differential amplifier are in each case connected to the output of the
sense amplifiers of the associated bit lines. This memory cell configuration
is preferably likewise used as an associative memory, the memory elements in
the two bit lines which are connected to the same word line in each case being
programmed complementarily with respect to one another. During read-out, there
is formed on one bit line the complementary signal of the other. The output
signal is formed from these complementary signals in the differential
amplifier. This differential method considerably improves the interference
immunity in respect of processed fluctuations.

Brief Summary Text - BSTX (27):
The construction and method of operation of the invention, however, together
with additional objects and advantages thereof will be best understood from the
following description of specific embodiments when read in connection with the
accompanying drawings.

Drawing Description Text - DRTX (2):
FIG. 1 is a diagram showing the architecture of an MRAM configuration;